

FIG. 1

# Initialization

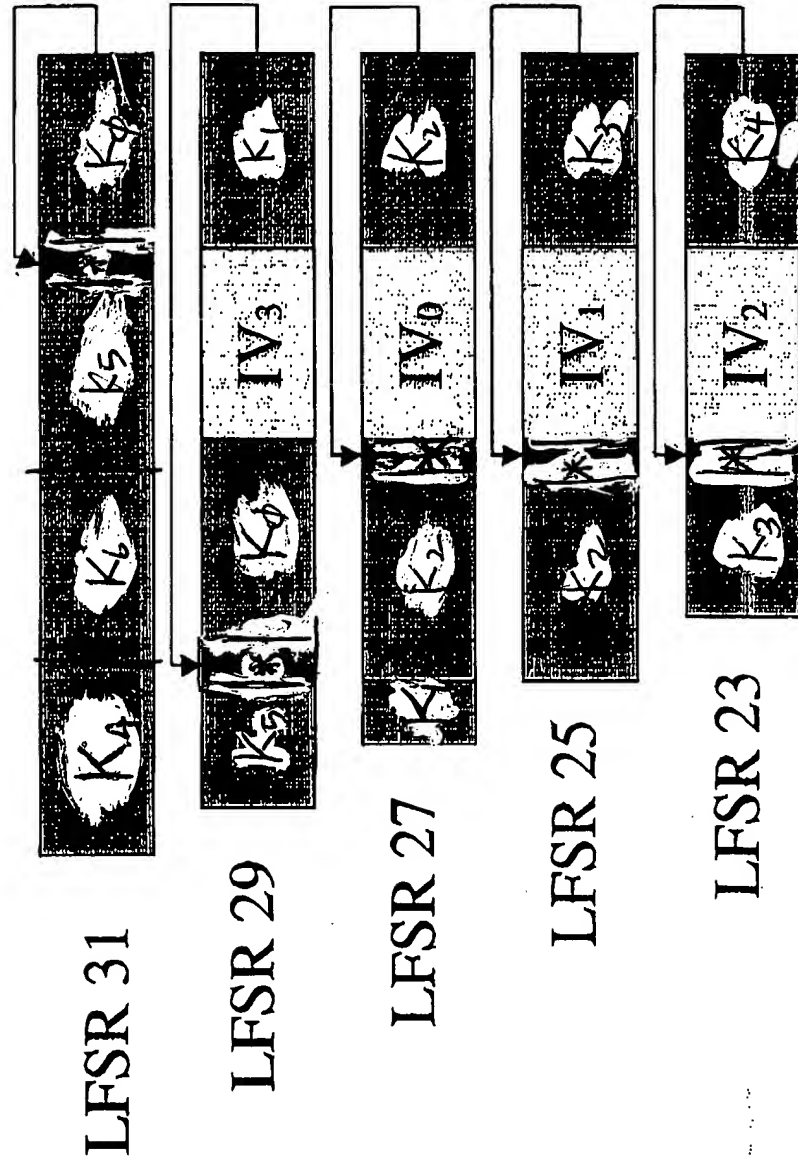


Fig. 2

\* Least significant bit of register is complemented

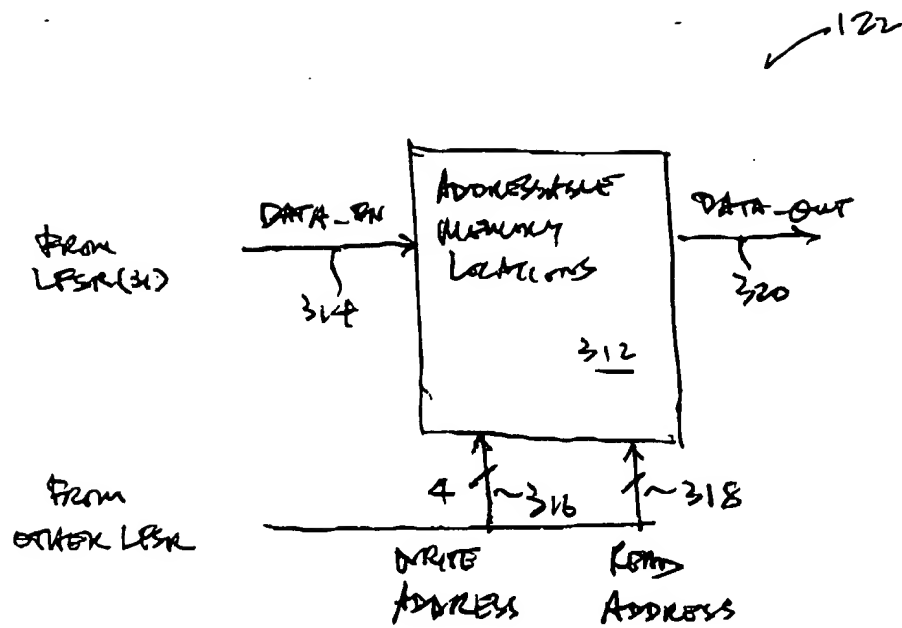


Fig. 3a

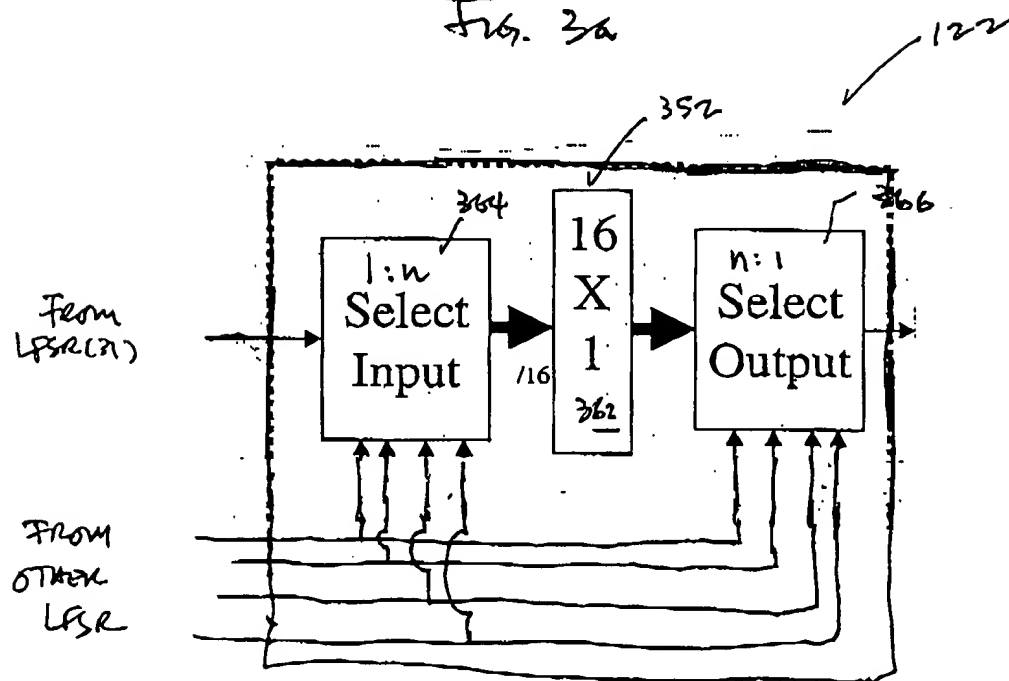


Fig. 3b